Webinar Invitation

Secure your IP and Revenue with FPGA Lock

Wednesday, 30. 10. 2024 (9 a.m. to 10:10 a.m.) – online

With the TEC BYTES webinars, TRS-STAR offers you bite-sized technical tidbits. TRS-STAR customers are cordially invited to this free training opportunity.

FPGA Lock is a small FPGA IP core that prevents overbuilding and cloning of your FPGA-based systems and consequently protects your revenue. It can also be used to guarantee hardware integrity in Safety Critical, Medical or Military/Defence applications.

The IP core uses less than 1 kLUT FPGA resources, one user IO and hardly any PCB realestate. It is intended to communicate with Microchip's ATSHA204A hardened crypto authentication IC. Users can prevent IP theft and Overbuilding.

The FPGA Lock IP uses symmetric cryptography, meaning the FPGA Lock IP and the crypto chip share a common secret key. In this webinar we will use the **T* Square Education Board** (available for just 59,99 €) for demonstration purposes. You can reproduce the webinar demo with this board using the free evaluation version of FPGA Lock IP.

Speaker:	Nial Steward (CEO Nial Steward Ltd.) Andreas Schwarztrauber (CEO TRS-STAR)
Language:	English
Prerequisites:	Technical understanding, basic knowledge of VHDL is desirable but not required. T* Square Education Board for customers who want to reproduce the hands-on afterwards..
Seminar form:	Presentation, hands-on at your own time and pace
Contact:	Andreas Schwarztrauber, (e-Mail: asc@trs-star.com) , +49 172 721 8963

Agenda (Zeitzone: CET)

09:00 a.m. – 09:05 a.m.	Welcome and introduction (Andreas Schwarztrauber)
09:05 a.m. - 09:15 a.m.	T*Square Education Boards (Andreas Schwarztrauber)
09:15 a.m. - 09:30 a.m.	Introduction to Cryptography (Nial Steward)
09:30 a.m. – 9:45 a.m.	Overview on FPGA Lock IP (Nial Steward)
09:45 a.m. – 10:00 a.m.	FPGA Lock Hands-On Demo (Nial Steward)
10:00 a.m. – 10:10 a.m.	Questions and answers

Register