TRS-STAR

P2L2 GmbH
programming & logic

Introduction to FPGA Design with Efinix

TEC BYTES Webinar

Dr. Markus Pfaff

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Agenda

- Efinity Overview
  - and how it is different from the crowd: Core + Periphery
- Webinar Project: Swell LED
- Efinity Toolflow
  - Project Setup
  - Interface Designer
  - Synthesis, PnR
  - Reports on Resources and Timing
  - Floorplanner
  - Programmer for FPGA Configuration

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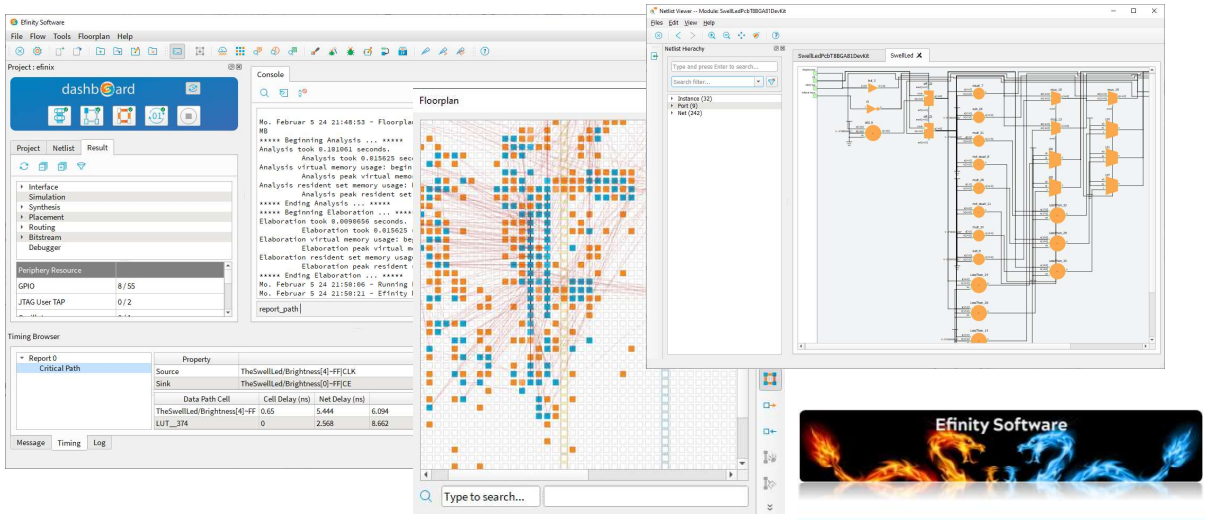
Efinity: Efinix FPGA Design Software Tool Suite



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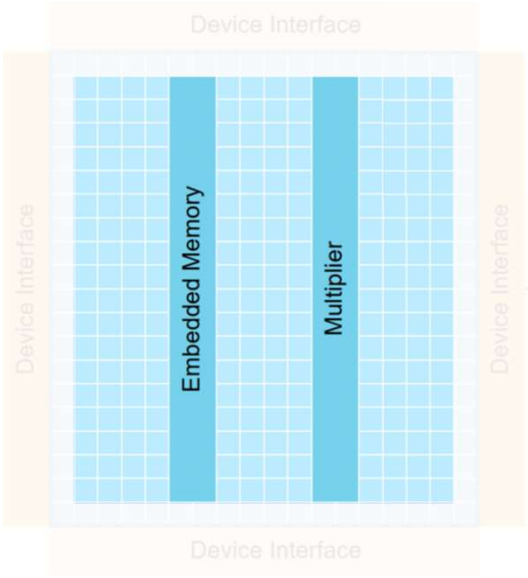
FPGA Design = Core + Periphery



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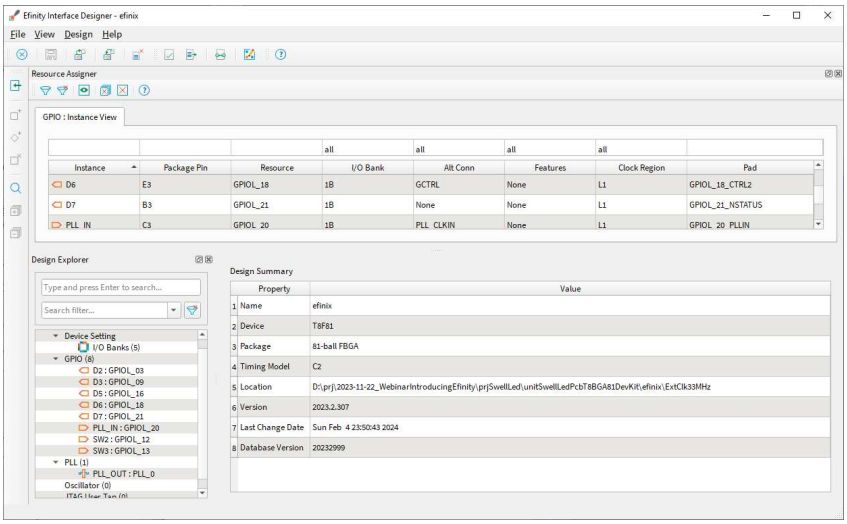
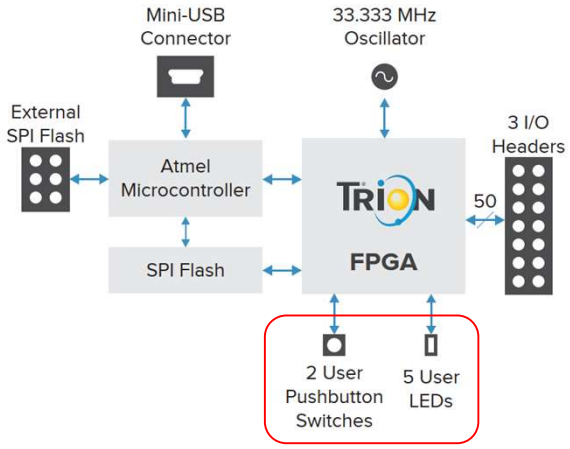
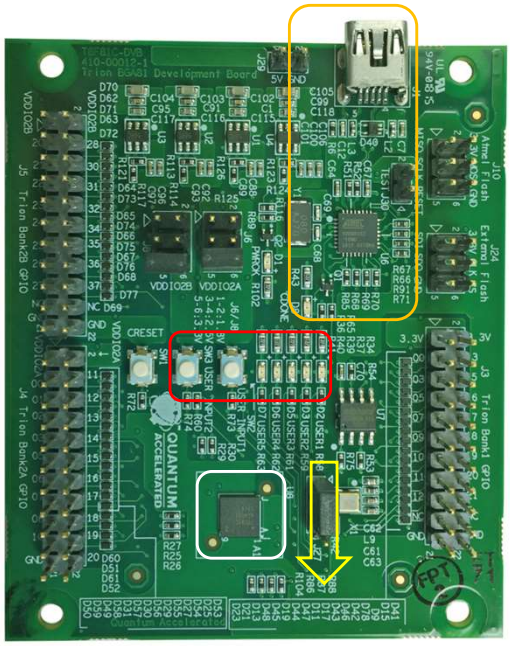
Efinity Interface Designer



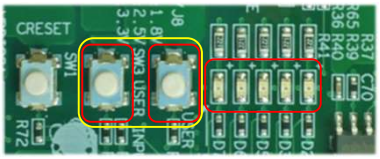
Trion T8BGA81 DevKit





Webinar Project: Swell LED - Specification

- A few LEDs mounted in a row
  - Brightness of the LEDs can be set by the user via:
- BrightenKey, which slowly brightens LEDs,
- DimmKey, which slowly dimms LEDs or
- Both Keys to dimm faster.
- Dimm speed raises from LED to LED



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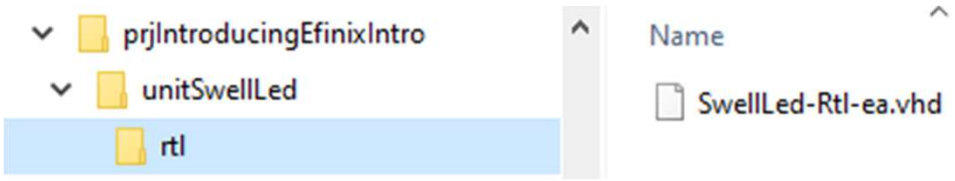
Project File Structure: RTL-Code



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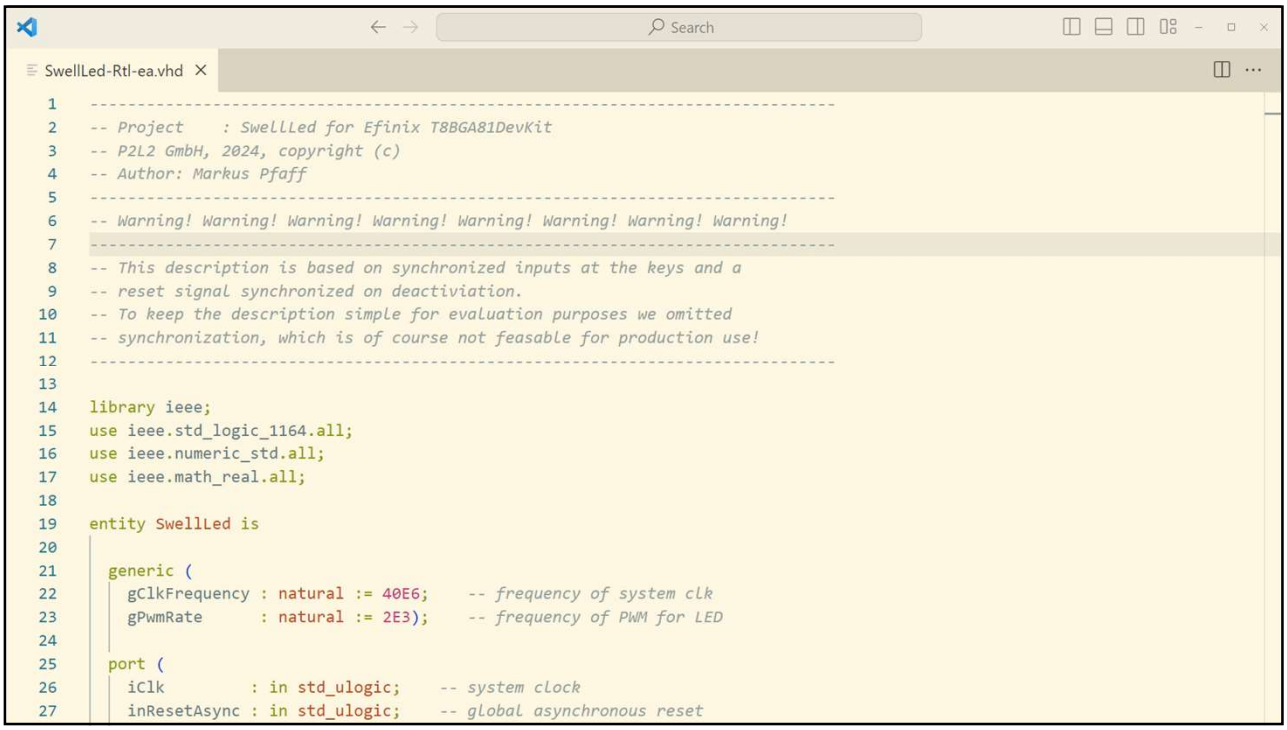

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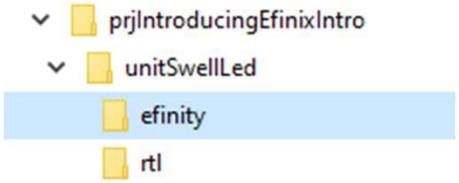
Project File Structure: efinity



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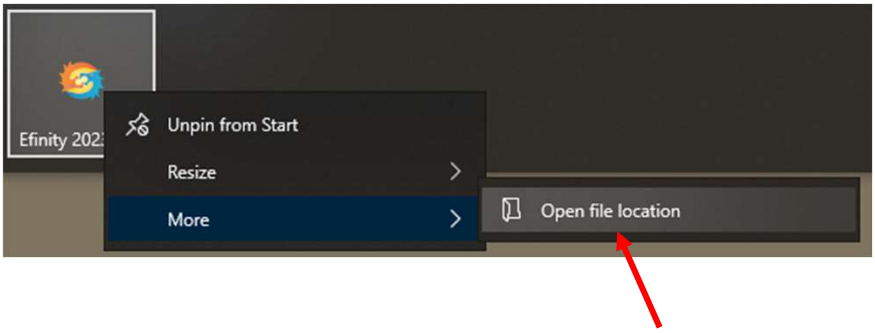
Preparing the Efinity Shortcut

In Windows Start Menu use the right mouse button to navigate to the the file location:



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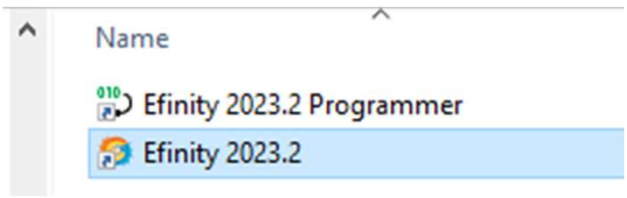
Preparing the Efinity Shortcut

This opens Windows Explorer at this place:



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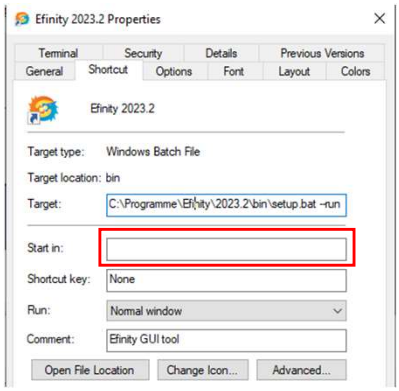
Preparing the Efinity Shortcut



Clear content of field
“Start in:”

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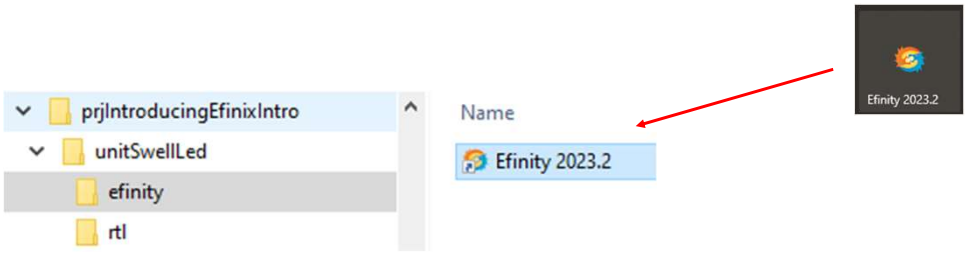
Using the Tailored Shortcut

Dragg and drop the Windows start icon into the project folder



This creates a link to the original shortcut

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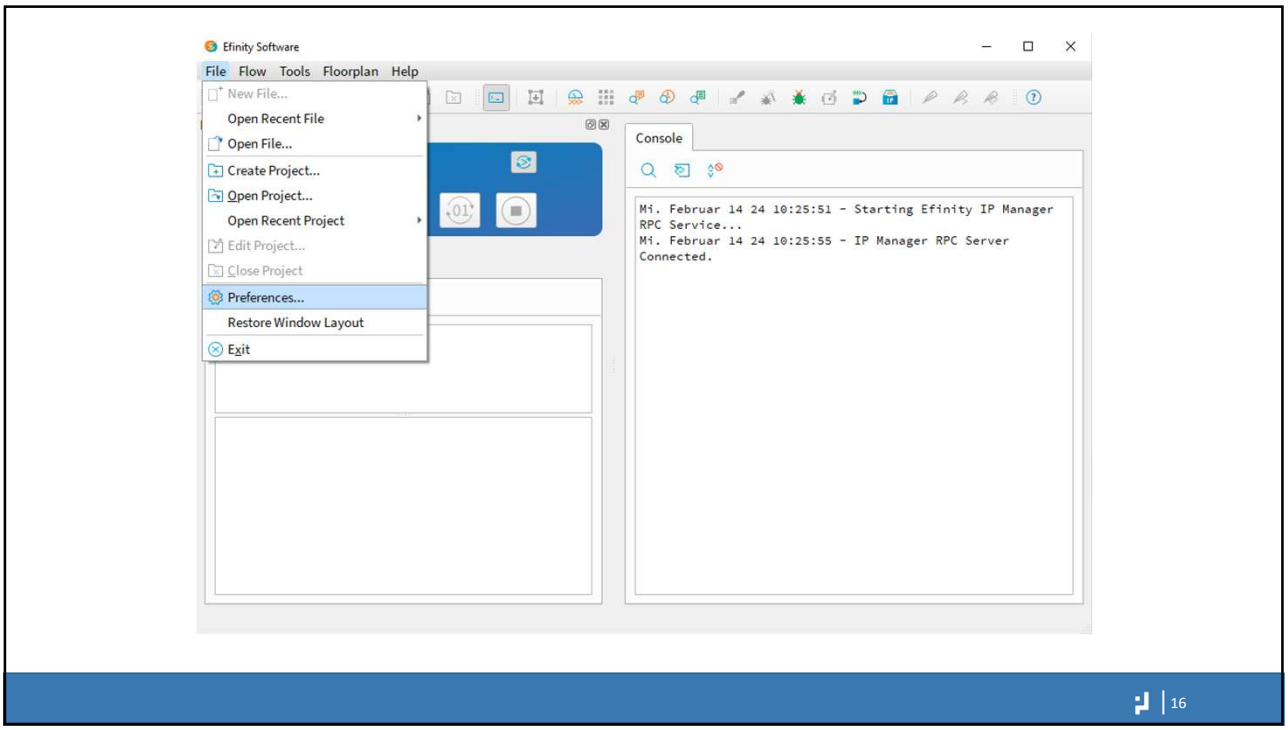
Efinity Software
File Flow Tools Floorplan Help
New File...
Open Recent File
Open File...
Create Project...
Open Project...
Open Recent Project
Edit Project...
Close Project
Preferences...
Restore Window Layout
Exit
Console
Mi. Februar 14 24 10:25:51 - Starting Efinity IP Manager RPC Service...
Mi. Februar 14 24 10:25:55 - IP Manager RPC Server Connected.
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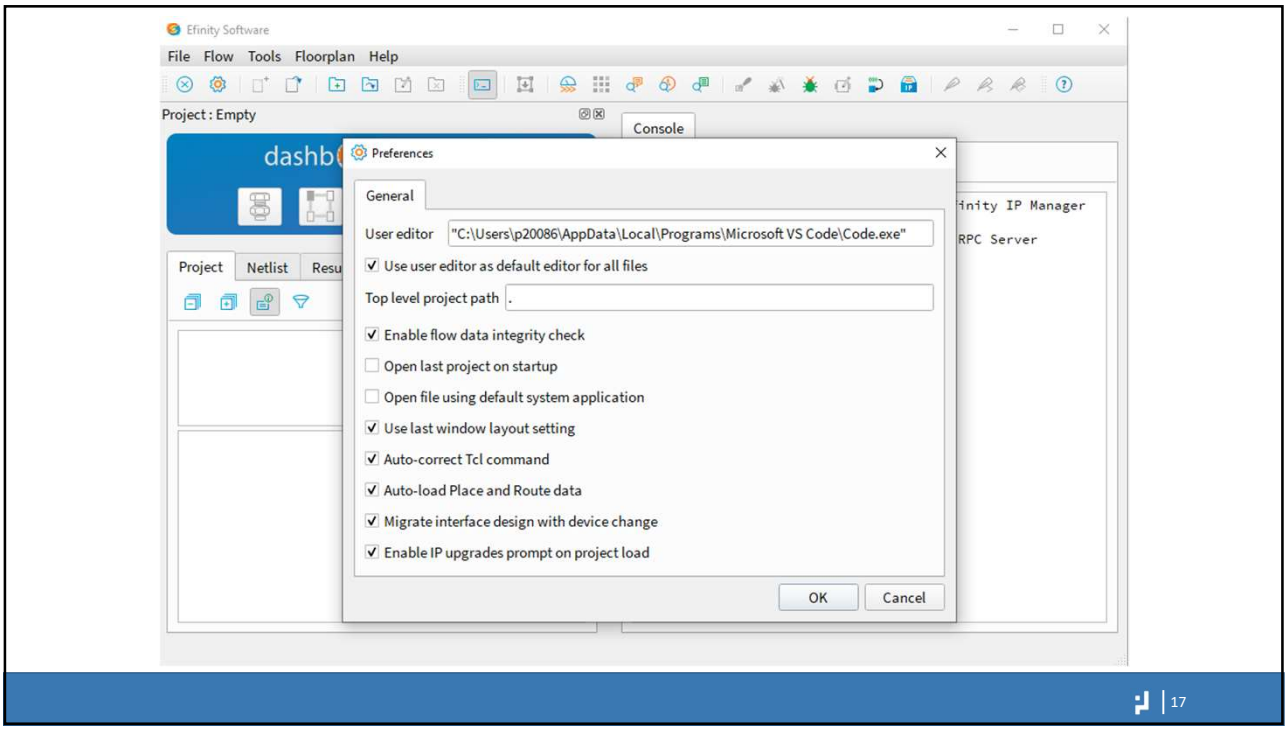
Efinity Software
File Flow Tools Floorplan Help
Project : Empty
Console
Preferences
General
User editor
"C:\Users\p20086\AppData\Local\Programs\Microsoft VS Code\Code.exe"
Use user editor as default editor for all files
Top level project path
.
Enable flow data integrity check
Open last project on startup
Open file using default system application
Use last window layout setting
Auto-correct Tcl command
Auto-load Place and Route data
Migrate interface design with device change
Enable IP upgrades prompt on project load
OK
Cancel
Project
Netlist
17

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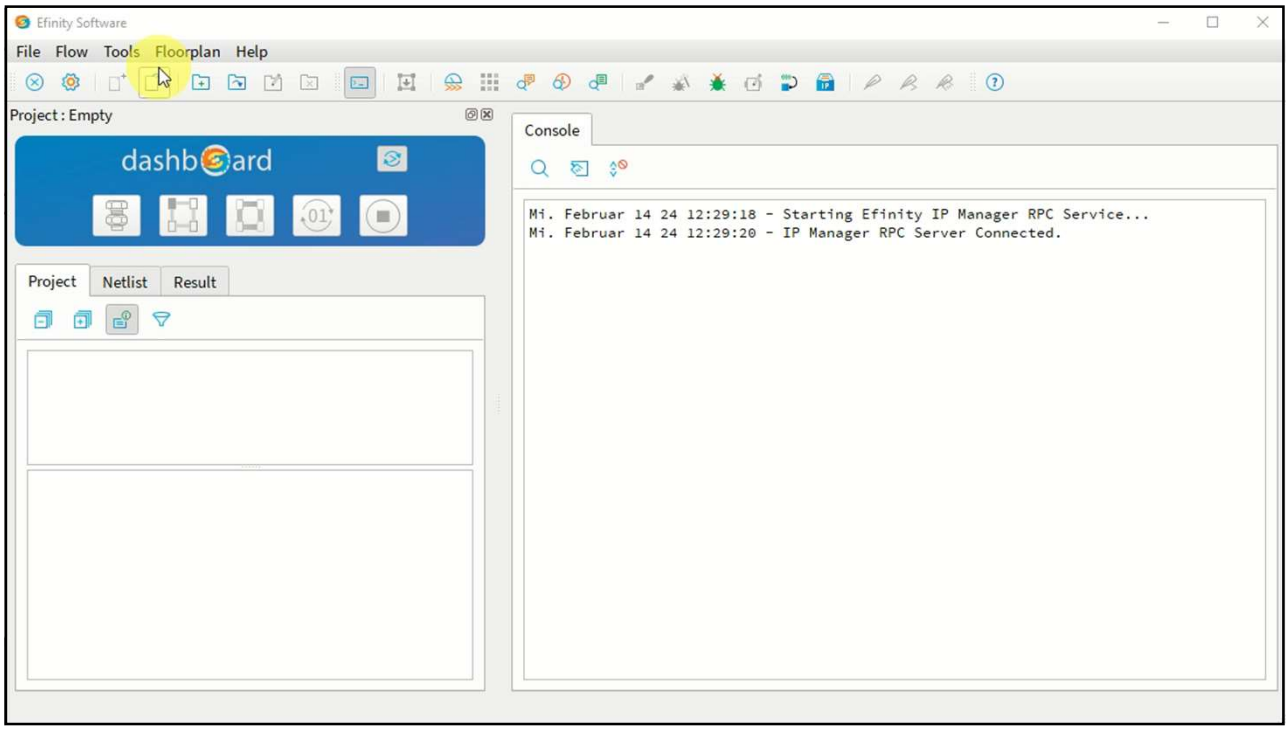
Efinity Software
File Flow Tools Floorplan Help
Project : Empty
dashboard
Project Netlist Result
Console
Mi. Februar 14 24 12:29:18 - Starting Efinity IP Manager RPC Service...
Mi. Februar 14 24 12:29:20 - IP Manager RPC Server Connected.

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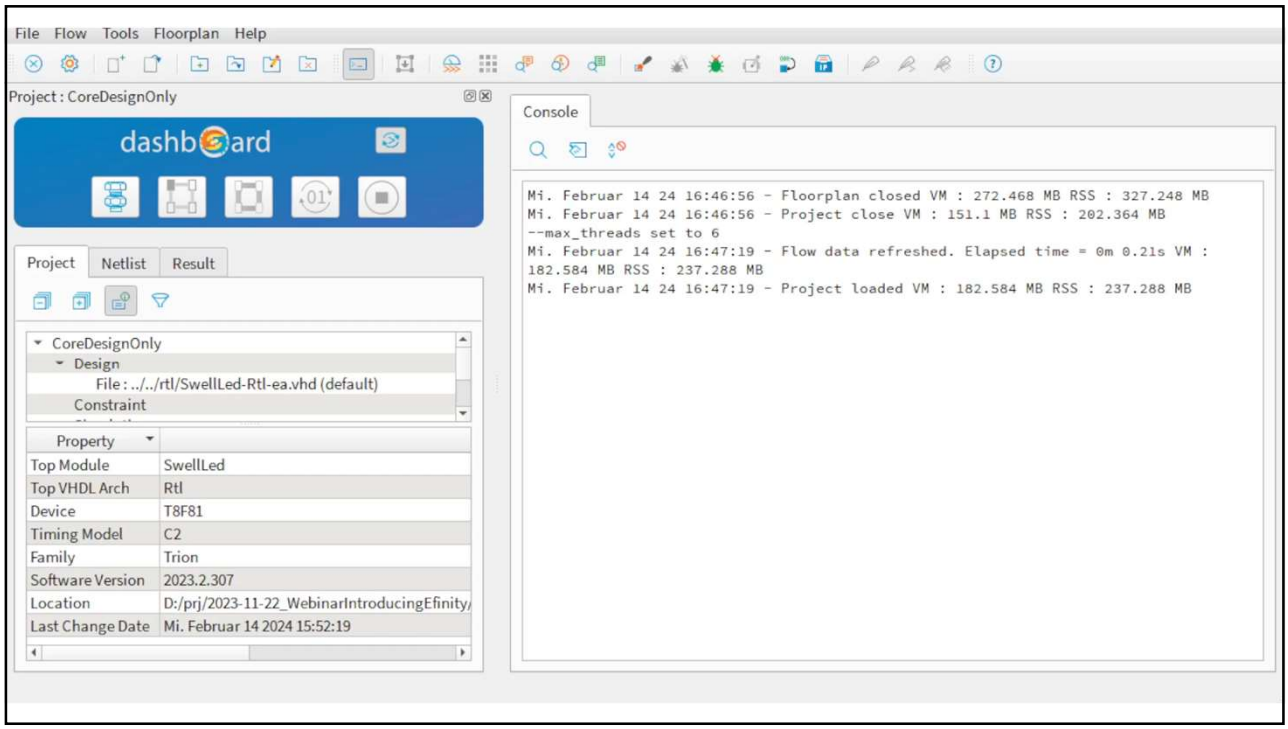
File Flow Tools Floorplan Help
Project : CoreDesignOnly
dashboard
Project Netlist Result
CoreDesignOnly
Design
File : ../../rtl/SwellLed-Rtl-ea.vhd (default)
Constraint
Property
Top Module SwellLed
Top VHDL Arch Rtl
Device T8F81
Timing Model C2
Family Trion
Software Version 2023.2.307
Location D:/prj/2023-11-22_WebinarIntroducingEfinity/
Last Change Date Mi. Februar 14 2024 15:52:19
Console
Mi. Februar 14 24 16:46:56 - Floorplan closed VM : 272.468 MB RSS : 327.248 MB
Mi. Februar 14 24 16:46:56 - Project close VM : 151.1 MB RSS : 202.364 MB
--max_threads set to 6
Mi. Februar 14 24 16:47:19 - Flow data refreshed. Elapsed time = 0m 0.21s VM : 182.584 MB RSS : 237.288 MB
Mi. Februar 14 24 16:47:19 - Project loaded VM : 182.584 MB RSS : 237.288 MB

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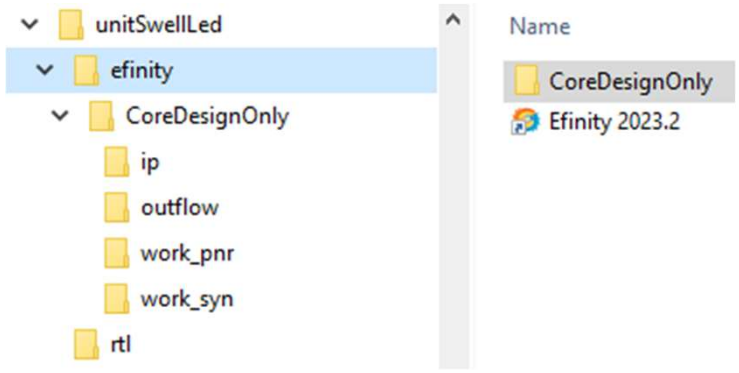
Current Directory Structure



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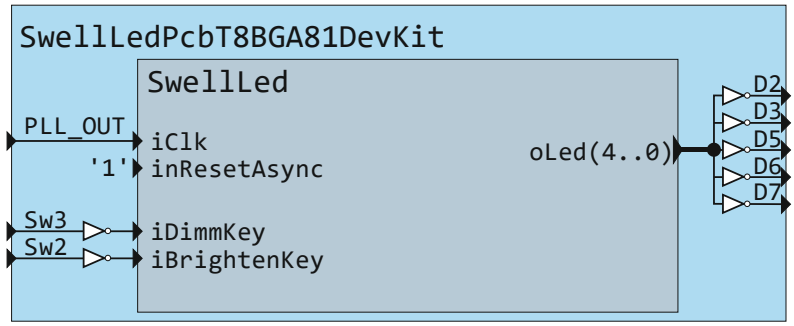
PCB-Adapter: A VHDL Wrapper



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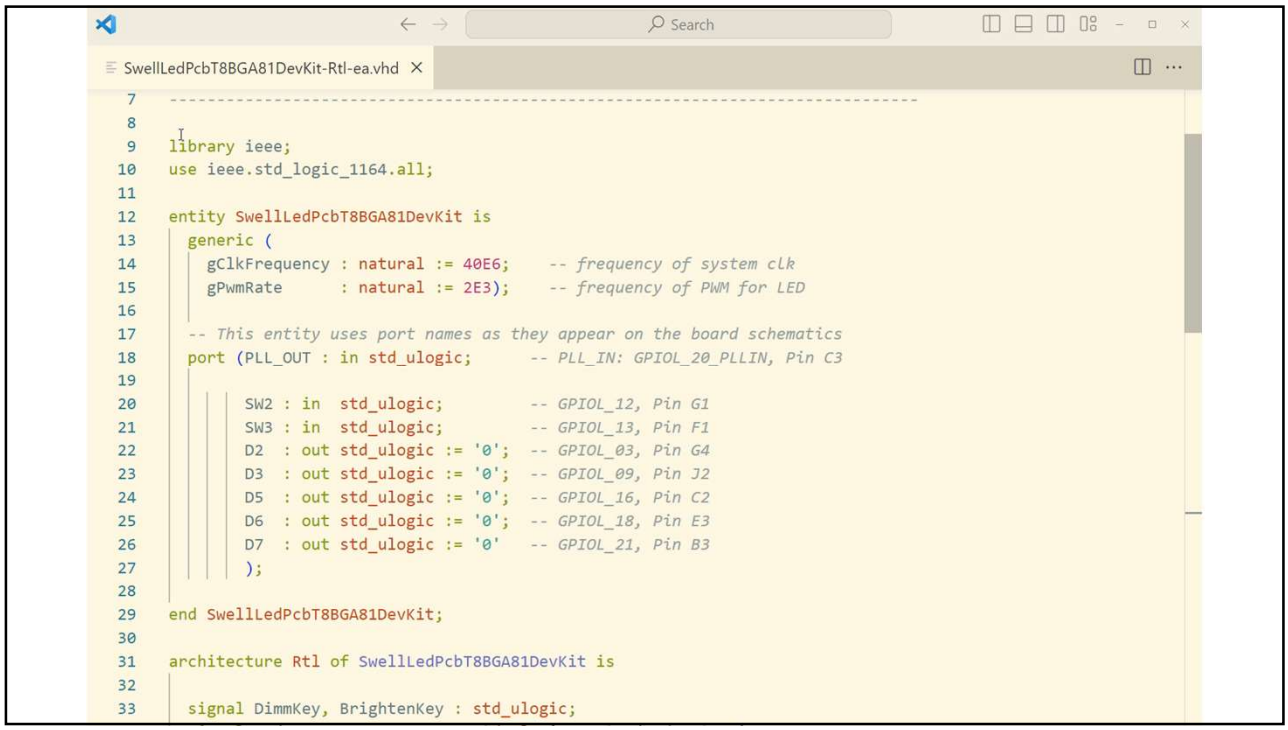

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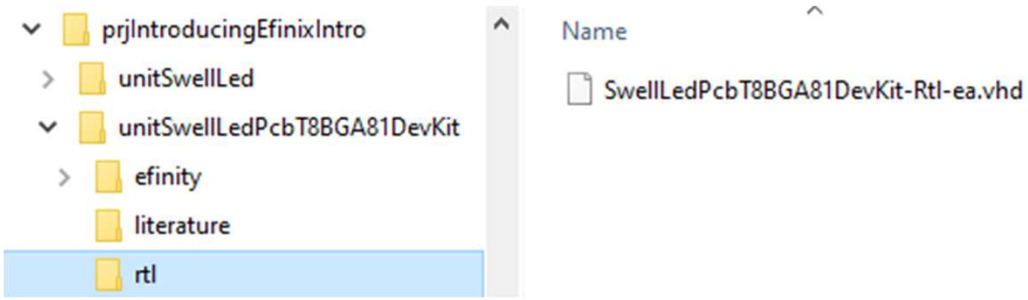
SwellLed + PCB Adapter



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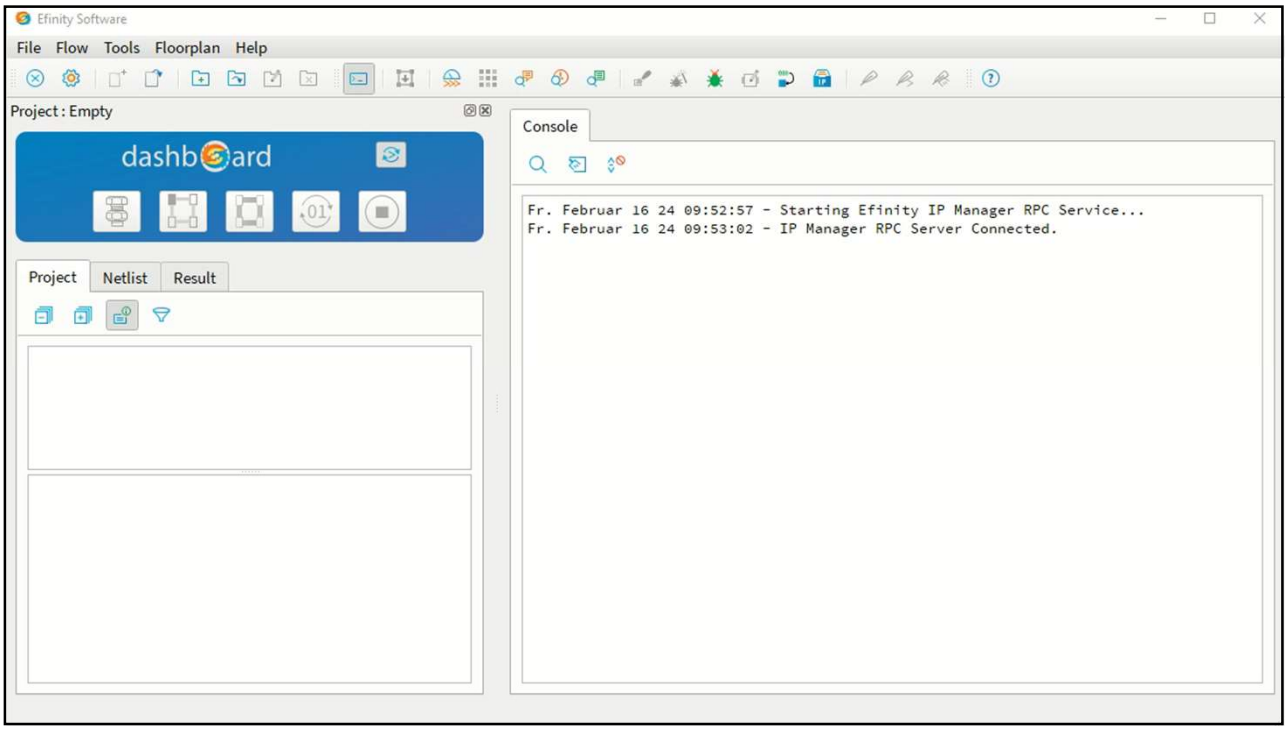
Efinity Software
File Flow Tools Floorplan Help
Project : Empty
dashboard
Project Netlist Result
Console
Fr. Februar 16 24 09:52:57 - Starting Efinity IP Manager RPC Service...
Fr. Februar 16 24 09:53:02 - IP Manager RPC Server Connected.

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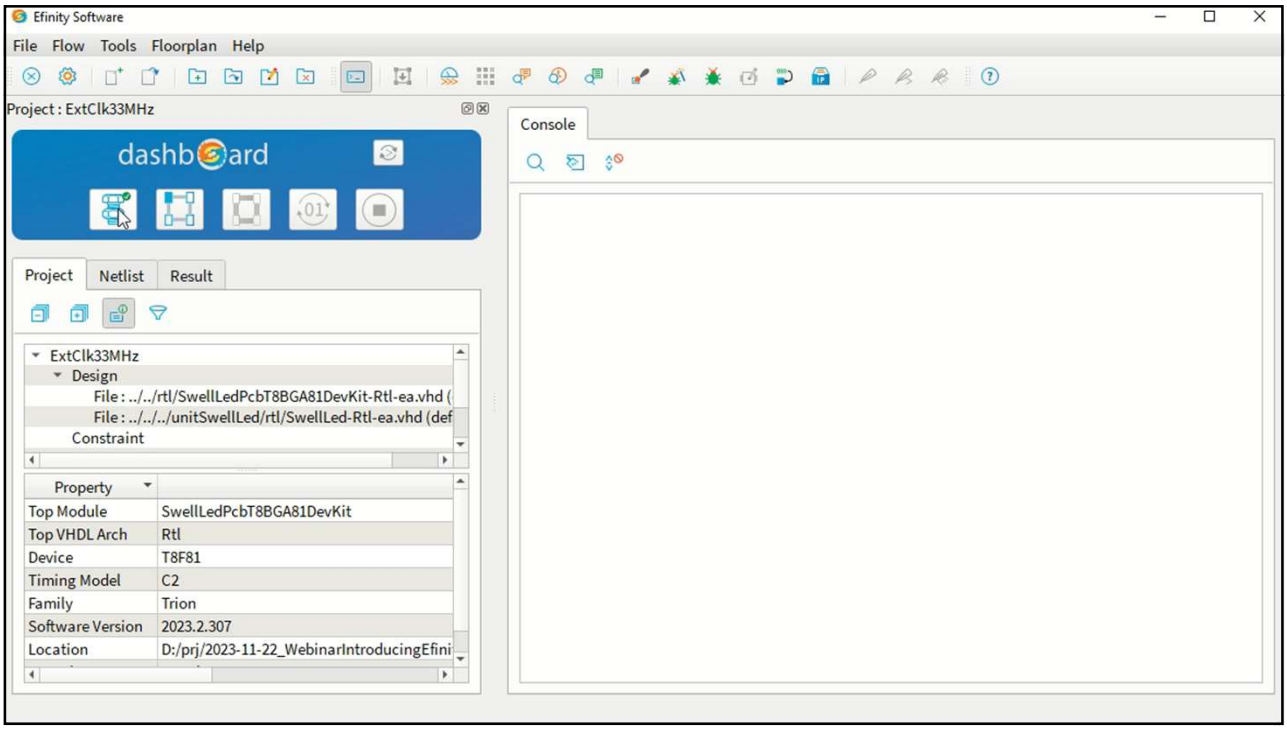
Efinity Software
File Flow Tools Floorplan Help
Project : ExtClk33MHz
dashboard
Project Netlist Result
Console
ExtClk33MHz
Design
File : ../../rtl/SwellLedPcbT8BGA81DevKit-Rtl-ea.vhd (
File : ../../../unitSwellLed/rtl/SwellLed-Rtl-ea.vhd (def
Constraint
Property
Top Module SwellLedPcbT8BGA81DevKit
Top VHDL Arch Rtl
Device T8F81
Timing Model C2
Family Trion
Software Version 2023.2.307
Location D:/prj/2023-11-22_WebinarIntroducingEfini

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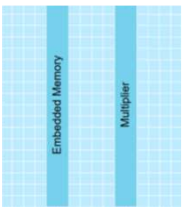
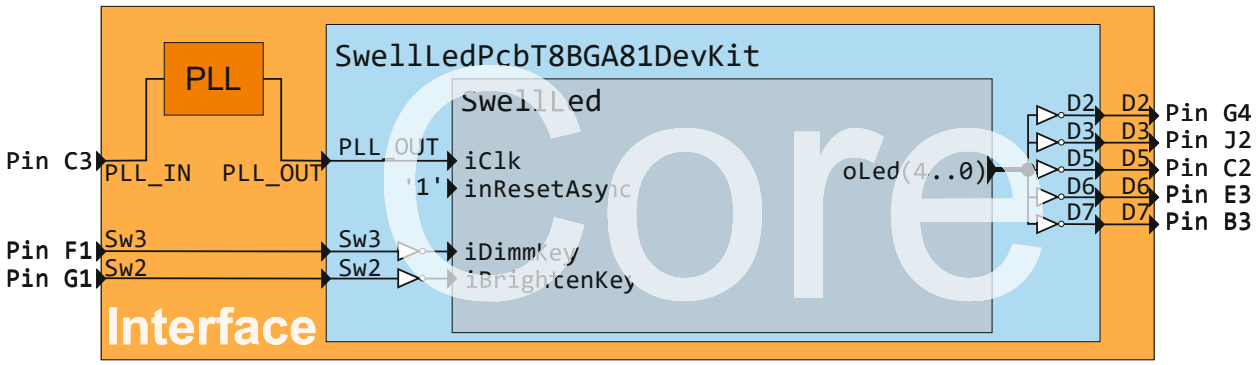
Adding the Interface Definition





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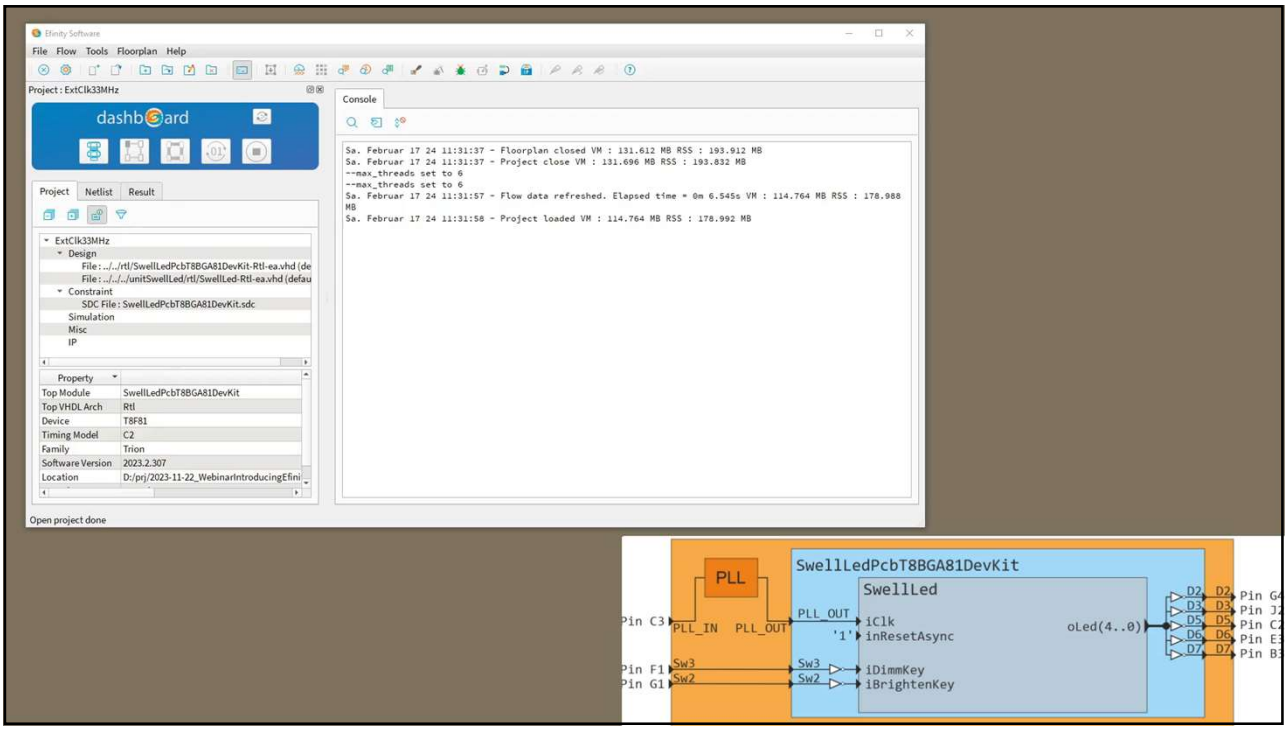

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Versioning your Files e.g. using Git

- Efinity User Guide, Section „Appendix: Efinity Project Files“
  - Files to include in version control
    - <project>.xml
    - <project>.peri.xml
    - <project>.sdc
    - debug_profile.wizard.json
    - dbg_top.v
    - <module>.v
    - settings.json

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VS Code for FGPA Design: VHDL by HGB

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Introducing Efinix Efinity FPGA Designflow

Dr. Markus Pfaff

Webinar

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