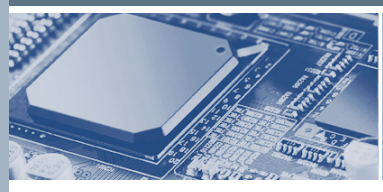


Topaz FPGAs

Low Power | High Volume | High Performance

Dear Customer,

Efinix recently announced the Topaz FPGA family. Topaz FPGAs are delivering high performance and low power in a cost-effective footprint for mainstream applications.

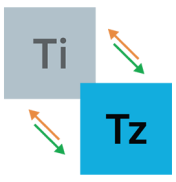
Topaz FPGAs combine an extra efficient architecture with the features and protocols most commonly used today (such as PCIe Gen 1-3, MIPI, LPDDR4, and LVDS).

Topaz FPGAs feature the innovative Quantum® compute fabric on an efficient, low-power, 16 nm process node. With this fabric, the Efinity software can pack more logic into the XLR cells, which means you can fit even more logic into the FPGA. Positioned for volume production applications, Topaz FPGAs let you do more for less.

Get your Topaz FPGA-Design started today!
Although Hard- and Software Support are not available as of today, you can get your Topaz FPGA-Design started today anyway: simply use a pin-compatible Titanium device!

There will be a seamless migration path between Titanium and Topaz enabling customers to start Topaz-Designs right away and switching to Topaz for production.

Contact fpga@trs-star.com for more details.



For details please refer to the latest Topaz family overview:

Topaz family overview

How cool is low-Power?

The photo shows the Ti375 running PCIe Gen4x4 and registering 29° C on a temperature monitor.

Learn about using the Titanium Power Estimator:

Titanium Power Estimator Manual

Upcoming TEC BYTES FPGA-webinars

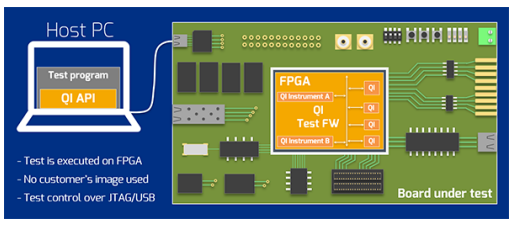
With the TEC BYTES webinars, TRS-STAR offers you bite-sized technical tidbits. TRS-STAR customers are cordially invited to this free training opportunity.

Testonica and TRS-STAR jointly present:

September 11th:

Introduction to Quick Instruments - a test framework for FPGA board quality control

Quick Instruments (QI) is a test & measurement framework that loads itself into on-board FPGAs for test, validation or programming purposes. The role of instruments is to verify PCBA hardware infrastructure: on-board interconnections and communication with peripheral components. In this way, every PCBA board can be checked for defects and stability issues. All instruments are pre-compiled for a target board and are being executed from a test platform using predefined templates. QI can be used for both FPGA-PCBA bring-up as well as end test in a production line. **When using QI there is no need to have your FPGA-Design ready for PCBA testing and there is no need to expose your FPGA-Design to a third party.**



Agenda

Register

Neil Steward Ltd. and TRS-STAR jointly present:

September 25th:

Secure your IP and Revenue with FPGA Lock

FPGA Lock is a small FPGA IP core that prevents overbuilding and cloning of your FPGA-based systems and consequently protects your revenue. It can also be used to guarantee hardware integrity in Safety Critical, Medical or Military/Defence applications.

The IP core uses less than 1 kLUT FPGA resources, one user IO and hardly any PCB realestate. It is intended to communicate with Microchip's ATSHA204A hardened crypto authentication IC. Users can prevent IP theft and Overbuilding.

The FPGA Lock IP uses symmetric cryptography, meaning the FPGA Lock IP and the crypto chip share a common secret key.
In this webinar we will use the T* Square Education Board **(available for just 59,99 €)** for demonstration purposes. You can reproduce the webinar demo with this board using the free evaluation version of FPGA Lock IP.

Agenda

Register

Meet us in person

Quick start

New to Efinix?
Just use our „Quick Start" to get your Efinix design started today!

More information:

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