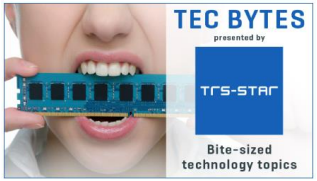
Components & System Solutions

Einstieg in den Efinix FPGA-Designflow



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TRS-STAR Mission Statement

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To guide and assist our customers and help them to get their electronic systems to market as fast as possible and enjoy our work

Services – Programmable Logic

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Together with our partner network we provide an ever increasing list of services around Efinix FPGAs

- Consulting and Training
- Eval-Boards and Samples
- FPGA SoMs for Rapid Prototyping or low volume production
- Customization of SoMs
- FPGA Design Services & Troubleshooting
- Schematic & Layout Reviews
- SiP (System in Package) Programming
- AES Encryption for IP security

P2L2 GmbH
programming & logic

TRS-Star Partner-Network

“Life is 10% about what you know and 90% about who you know”

Efinix in a nutshell

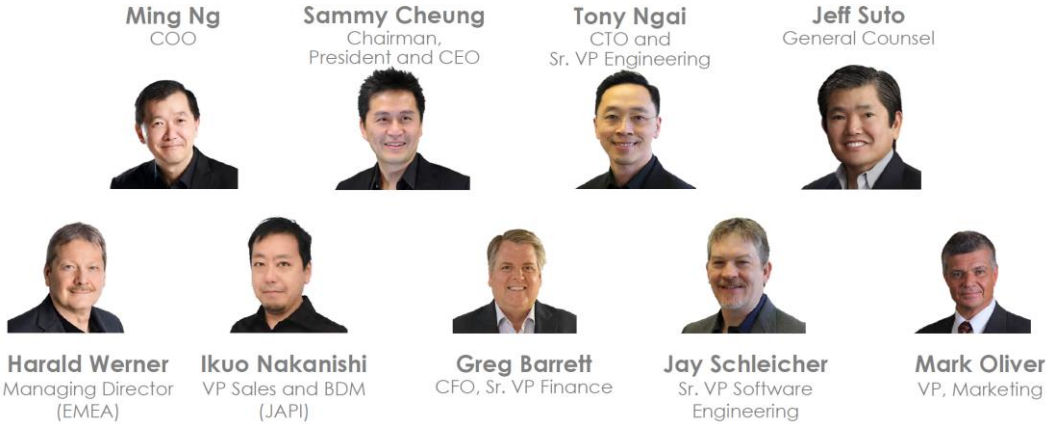
Facts

- Fabless FPGA vendor
- Worldwide Presence with 200+ employees
- EMEA HQ: Munich
- AE Office: Manchester

Company History

- Founded in 2012
- Inventor of **Quantum™** accelerated eFPGAs
- 2018 Trion FPGAs (40 nm CMOS, SMIC)
- 2020 TRS-STAR Distributor in EMEA, now #1
- 2022 Titanium (16 nm CMOS, TSMC)

Executive Leadership



Disruptive FPGA technology

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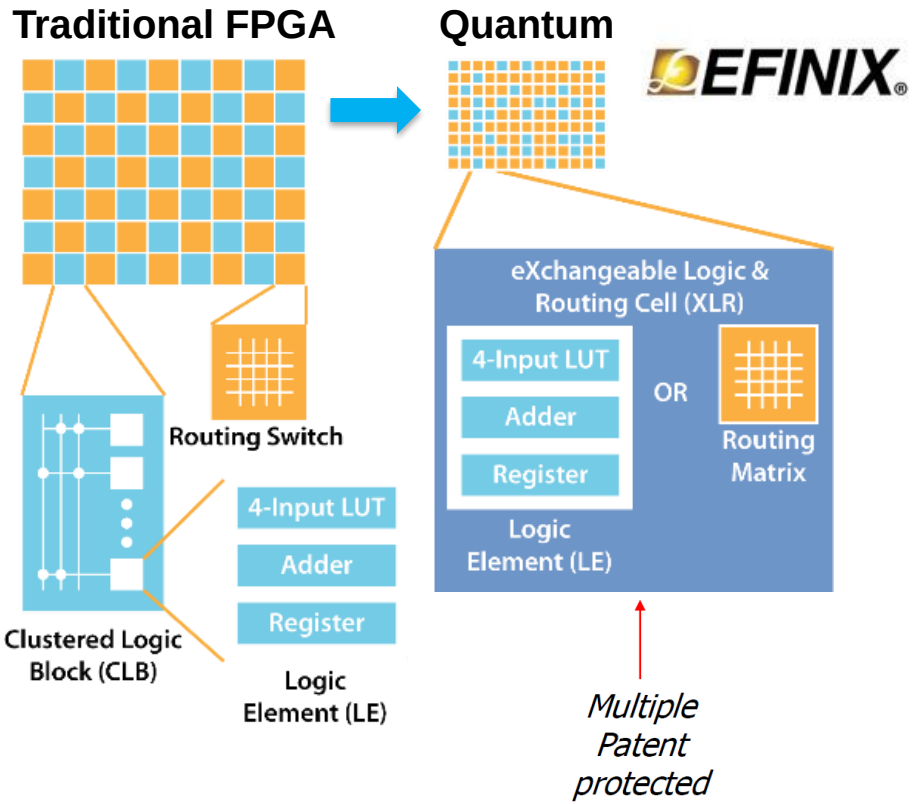
Quantum FPGA Technology from Efinix

XLR e**X**changeable **L**ogic or **R**outing Cell
(the decision is made at compile time)

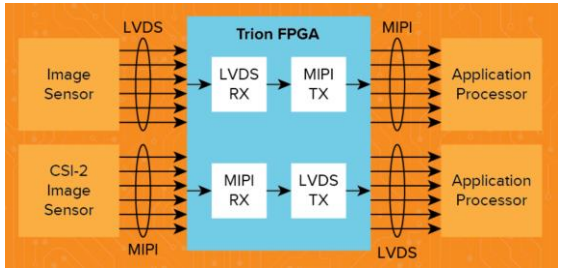
Resulting in Advantages over traditional FPGAs

- Optimal resource usage -> smaller dies
  - ✓ Cost benefit
  - ✓ Small packages -> less PCB real estate -> compact systems
  - ✓ Less transistors, shorter routing -> **less Power Consumption** -> less cost
- 7 layers of metal vs.12+ layers -> reduced NRE cost
  - ✓ Cost benefit, **more flexibility to adjust to customer needs**
- Single architecture scalable to 1 Mio+ LEs
- Standard process and Silicon process agnostic
  - ✓ Could be transferred to other fabs
  - ✓ **Short Leadtimes, even during allocation!**



Trion FPGA Family

- 40 nm CMOS, SMIC standard process
- Scales from 4 to 120 kLUT
- Optional MPM (NRE cost)
- T4/T8 offer ultra-low Power process in certain packages
- MIPI D-PHY with 1.5 Gibt/s and build-in CSI-2 Controller
- RISC-V Softcore (Sapphire)
- Ideal for (but not limited to) camera applications



Trion FPGA Family

Feature	T4	T8	T13	T20	T35	T55	T85	T120
Logic Elements (LEs)	3,888	7,384	12,828	19,728	31,680	54,195	84,096	112, 128
Mask Programmable Memory (MPM)	✔	✔	✔	✔	–	–	–	–
Embedded RAM Bits (kb)	77	123	727	1,044	1,475	2,765	4,055	5,407
Embedded 5K RAM blocks	15	24	142	204	288	540	792	1,056
18x18 Multipliers	4	8	24	36	120	150	240	320
PLLs	1	5	5	7	7	8	8	8
LVDS (TX, RX)	–	6, 6	13, 13	20, 26	20, 26	52, 52	52, 52	52, 52
DDR3, LPDDR3, LPDDR2 (up to 1066 Mbps)	–	–	–	x16	x16	x32	x32	x32
MIPI 4-lane DPHY with built-in CSI-2 controller	–	–	2 RX 2 TX	2 RX 2 TX	2 RX 2 TX	3 RX 3 TX	3 RX 3 TX	3 RX 3 TX
Data sheet (PDF)								
Product page								

Trion Package Options

- IO-rich family with package options that allow pin-compatible scalability
- T4/T8 in 49/81 ball FBGA are using an ultra-low Power process
- The 100-pin LQFP has 16 Mbit SPI-Flash in the same package and is ideally suited to replace EOL (or expensive) CPLDs

Package	Pitch (mm)	Size (mm)	GPIO (1)	PLLs	SPI Flash (Mbit)	LVDS Pairs TX, RX	MIPI CSI-2 TX, RX (1)	DDR DRAM (1)	T4	T8	T13	T20	T35	T55	T85	T120
49-ball FBGA	0.4	3x3	33	1					✔	✔						
80-ball WLCSP	0.4	4.5x3.6	33	3			1, 1					✔				
81-ball FBGA	0.5	5x5	55	1					✔	✔						
100-pin LQFP	0.5	14x14	65	5	16	4, 4					✔	✔				
144-pin LQFP	0.5	20x20	97	5		6, 6				✔		✔				
169-ball FBGA	0.65	9x9	73	5		8, 12	2, 2				✔	✔				
256-ball FBGA	0.8	13x13	195	5		13, 13					✔	✔				
324-ball FBGA	0.65	12x12	130	7		20, 26	2, 2	x8, x16				✔	✔	✔	✔	✔
400-ball FBGA	0.8	16x16	230	7		20, 26		x8, x16				✔	✔			
484-ball FBGA	0.8	18x18	256	8		40, 40		x16, x32						✔	✔	✔
576-ball FBGA	0.65	16x16	278	8		52, 52	3,3	x16, x32						✔	✔	✔

(1) The MIPI and DDR interface have dedicated I/O; therefore; the GPIO number does not include the I/O count for those interfaces.

Titanium FPGA Family

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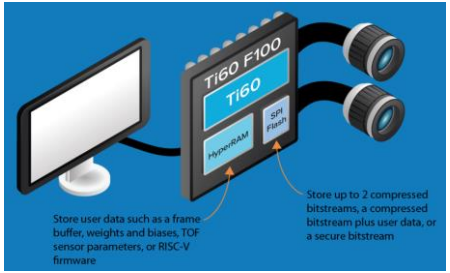
- 16 nm CMOS, TSMC standard process
- Scales from 35 kLUT to 1 Mio LUT
- Ti550 and higher are Roadmap Devices
- Excellent performance at low low-Power consumtion
- SEU detection and automatic recovery
- Support bitstream security
- MIPI D-PHY with 2.5 Gibt/s
- LPDDR4 support
- RISC-V Softcore (Sapphire)
- Sapphire Hardened RISC-V Quadcore for selected devices
- Ideal for (but not limited to) camera applications, sensors and edge devices

Feature	Ti35	Ti60	Ti90	Ti120	Ti135	Ti180	Ti200	Ti375	Ti550	Ti750	Ti1000
Logic Elements (LEs)	36,176	62,016	92,534	123,379	133,844	176,256	198,288	370,137	550,000	750,000	1,000,004
10K RAM blocks (Mb)	1.53	2.62	6.88	9.18	9.95	13.11	14.75	27.53	40.92	55.8	74.4
DSP blocks	93	160	336	448	486	640	720	1,344	2,006	2,736	3,648
PLLs	4	4	10	10	12	10	12	12	12	12	12
GPIO	34	34	80	80	181	80	181	181	200	200	200
High-speed I/O	146	146	232	232	235	232	235	235	320	320	320
LPDDR4/4x	–	–	x32	x32	2 x32	x32	2 x32	2 x32	2 x72	2 x72	2 x72
MIPI D-PHY 2.5 Gbps	–	–	4 RX 4 TX	4 RX 4 TX	3 RX 3 TX	4 RX 4 TX	3 RX 3 TX	3 RX 3 TX	3 RX 3 TX	3 RX 3 TX	3 RX 3 TX
16 Gbps Tranceivers	–	–	–	–	x16	–	x16	x16	x24	x24	x24
25.8 Gbps Transceivers	–	–	–	–	–	–	–	–	x8	x8	x8
Hardened RISC-V block	–	–	–	–	Quad Core	–	Quad Core	Quad Core	Quad Core	Quad Core	Quad Core
PCIe® Gen4 (16G)	–	–	–	–	2 x4	–	2 x4	2 x4	2 x8	2 x8	2 x8
Data sheet (PDF)											
Product page											

Titanium Package Options



- WLCSP allows integration of 60 kLUT-FPGA into small sensors, edge devices and wearables
- The 100-pin FBGA contains 35-60 kLUT FPGA, 16 Mbit SPI-Flash and 256 Mbit HyperRAM in a 5.5 mm x 5.5 mm package

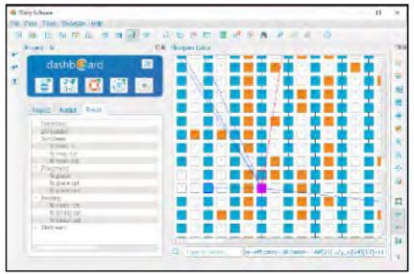
Package	Pitch (mm)	Size (mm)	Ti35	Ti60	Ti90	Ti120	Ti135	Ti180	Ti200	Ti375	Ti550	Ti750	Ti1000
64-ball WLCSP	0.4	3.5x3.4		✔									
100-ball FBGA	0.5	5.5x5.5	✔	✔									
225-ball FBGA	0.65	10x10	✔	✔									
361-ball FBGA	0.65	13x13			✔	✔		✔					
400-ball FBGA	0.8	16x16			✔	✔		✔					
484-ball FBGA	0.8	18x18			✔	✔		✔					
529-ball FBGA	0.8	19x19			✔	✔	✔	✔	✔	✔			
676-ball FBGA	0.8	22x22					✔		✔	✔			
900-ball FBGA	0.8	25x25					✔		✔	✔			
1,156-ball FBGA	1.0	35x35					✔		✔	✔	✔	✔	✔

Efinity® Integrated Development Suite

- Supports all Efinix-FPGAs from T4 to largest Ti
- Standard RTL-to-bitstream FPGA development tool
- Requires license (free of charge)
- Synthesis tool optimized for Quantum™ technology
- Two major releases per year: Efinity v<yyyy>.1 (June) and Efinity v<yyyy>.2 (December)

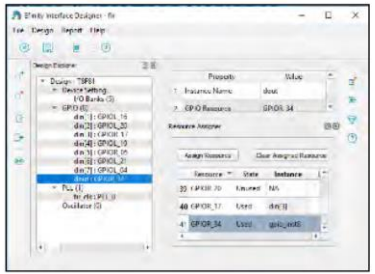
Core Designer

FPGA Core Fabric
(Synthesis, Place and Route)



Interface Designer

Subsystems
(I/O, DDR, MIPI, etc.)



Safety Critical Design with Efinix FPGAs

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Efinity v2023.1 and later meets requirements for SIL 4 / ASIL D

- The certificate and assessment report can be found on the exida SAEL (Safety Automation Equipment List). The SAEL is a regularly maintained list of instrumentation that is functional safety certified per exida standards for use in safety instrumented systems.

exida

The manufacturer may use the mark:

exida CERTIFIED FUNCTIONAL SAFETY

Revision 1.1 September 29, 2023
Surveillance Audit Due
September 1 , 2026

ANAB
ANSI National Accreditation Board
ACCREDITED
PRODUCT CERTIFICATION BODY
#1004

Certificate / Certificat
Zertifikat / 合格証

EFI 2207092 C001

exida hereby confirms that the:

Efinity® IDE and Toolchain v2023.1 and later

Efinix Technology (M) Sdn. Bhd.
Penang - Malaysia

Has been assessed per the relevant requirements of:
IEC 61508:2010 and ISO 26262:2018

and meets requirements providing a level of integrity to:
SIL 4 / ASIL D Qualified

Tool Functions:
The Efinity® IDE and Toolchain suite is an integrated development environment designed for Efinix FPGA development. Using Efinity, customers can develop, compile and test their FPGA design from RTL source code all the way down to bitstream programming on FPGA development boards.

Application Restrictions:
The tools of the Efinity® IDE and Toolchain must be used per the defined use cases, and all requirements specified for the tool users (conditions and assumptions of use) shall be fulfilled, as described in the Functional Safety Manual for each tool.

exida Certification

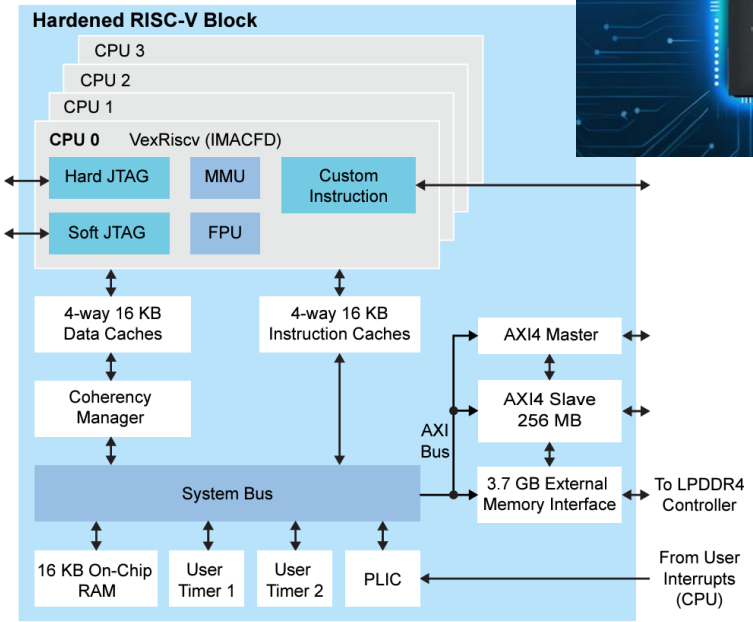
Jack Gao
Evaluating Assessor

Raymond Lee
Certifying Assessor

Page 1 of 2

Ti135/200/375: Quad-Core RV32 SoC

- CPU:
  - 6-stages pipeline in-order architecture
  - Instruction: IMACFD
  - Cache: I$ & D$, 4-ways 16KB each
  - **MMU, FPU, Branch Predictor support**
  - **Custom Instruction support**
- SoC:
  - **16KB on Chip RAM**
  - Hard Wired 256b AXI4 Ext. Memory to LPDDR4
  - 128b AXI Master @ 250MHz
  - 32b AXI Slave @ 250Mhz
  - 24 User Interrupts
  - CLINT timer, User timer, PLIC
- **CPU f_max = 1.0 GHz @ 500mW typical**
- **Linux & RTOS ready**

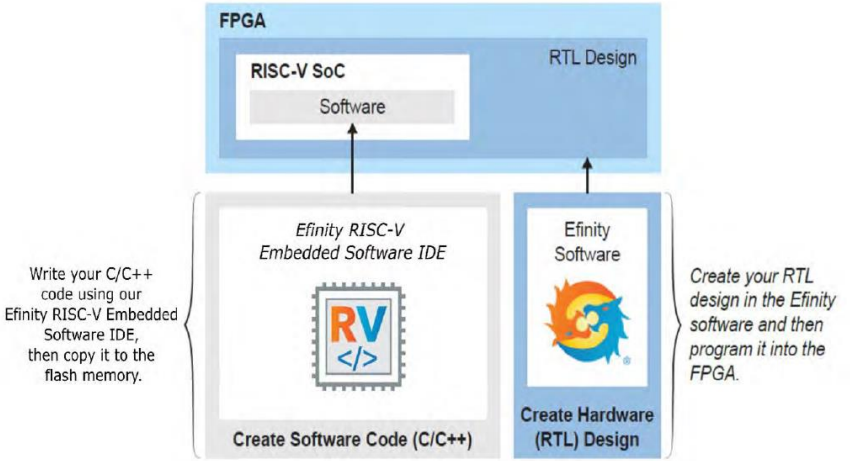


Efinity Tool-Suite for SoC Development

The Efinity Tool-Suite supports both the Hardned RISC-V Quadcore as well as the RV32 Soft-Core:

- Efinity ® software
- Pre-compiled, open-source SDK
- Eclipse IDE (Integrated Development Environment) for managing projects and software with Ashling GUI
- RISC-V GCC compiler and GDB debugger
- OpenOCD debugger for debugging applications
- Windows build tools (Windows)

https://www.efinixinc.com/products-riscv.html



Ti375 timeline

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Timeline:

- Efinity v2023.2 and later support Ti375
- January patch also supports Ti135/200
- Initial Package offering is C529
- June '24 Efinity v2024.1 - **stay tuned for exciting new Ti375 features!**

For more information get in touch with fpga@trs-star.com

Table 2: Ti375 Package-Dependent Resources

Resource		C529	N1156
Single-ended GPIO (Maximum)	HVIO LVCMOS: 1.8, 2.5, 3.0, 3.3 V LVTTL: 3.0, 3.3 V	51	103
	HSIO (1.2, 1.5, 1.8 V LVCMOS, HSTL, and SSTL)	176	234
Differential GPIO (Maximum)	HSIO (LVDS, Differential HSTL, and SSTL)	88	117
	HSIO (MIPI D-PHY Data Lanes)	77	100
	HSIO (MIPI D-PHY Clock Lanes)	11	17
LPDDR4 PHY with memory controller	x32 DQ width	1	2
MIPI D-PHY Hard Blocks	RX	-	3
	TX or SSC PLL	-	3
Global clock or control signals from GPIO pins		32	32
Fractional PLLs		12	12
SerDes transceivers	PCIe Gen4	-	up to 2
	Ethernet SGMII, and Ethernet 10GBase-KR, or PMA Direct	-	up to 4

Important: All specifications are preliminary and pending hardware characterization.

T*Square Education Boards

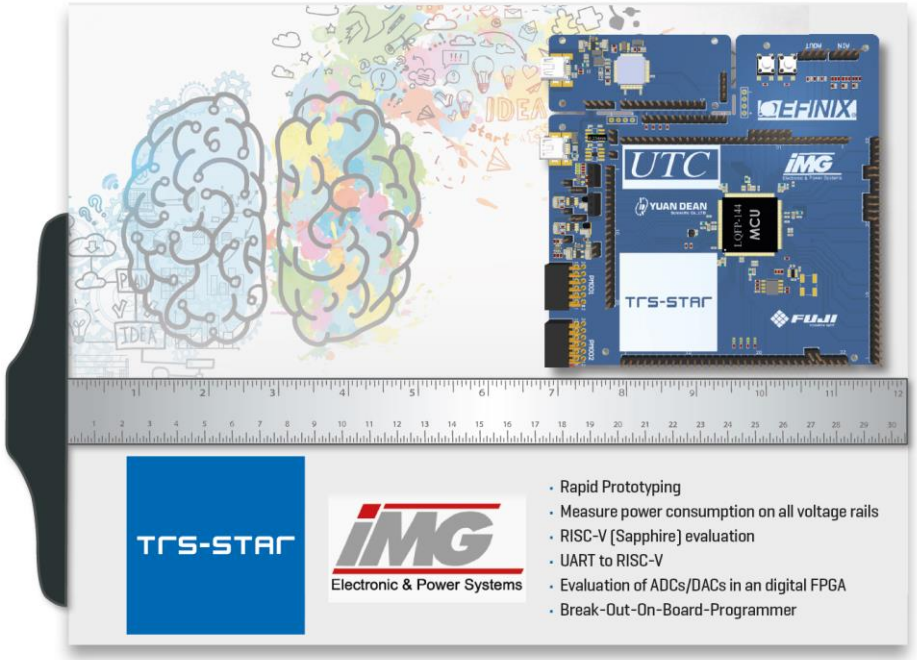
Timeline:

- April 2024: T*Square T20-100*
- April 2024: T*Square T20-144
- May 2024: T*Square Ti60-100**

  *) with 16 Mbit integrated SPI-Flash

  **) with 16 Mbit integrated SPI-Flash & 256 Mbit Hyper-RAM

- Rapid Prototyping
- Measure power consumption on all voltage rails
- RISC-V (Sapphire) evaluation
- UART to RISC-V
- Evaluation of ADCs/DACs in an digital FPGA
- Break-Out-On-Board-Programmer



Get you Efinix FPGA design started today

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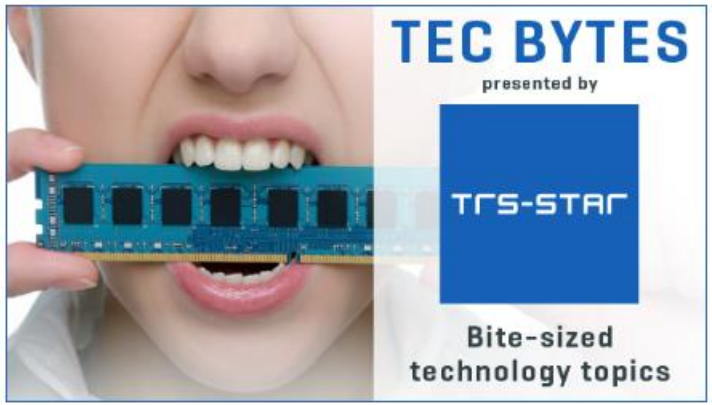
https://www.trs-star.com/en/products/fpga



Quick start

Efinity Software

Simple, Easy-to-Use Toolflow.
Free license now available!

Simulators

Contact TRS-STAR for special pricing on Aldec simulators.

Trainings & Webinars

The TRS-STAR YouTube channel „Tec Bytes“ contains a Design flow tutorial, that enables a quick start to the Efinity Design Software.
More interesting webinars can be found on: TRS-STAR Webinars

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T8 Board just 60,22 €

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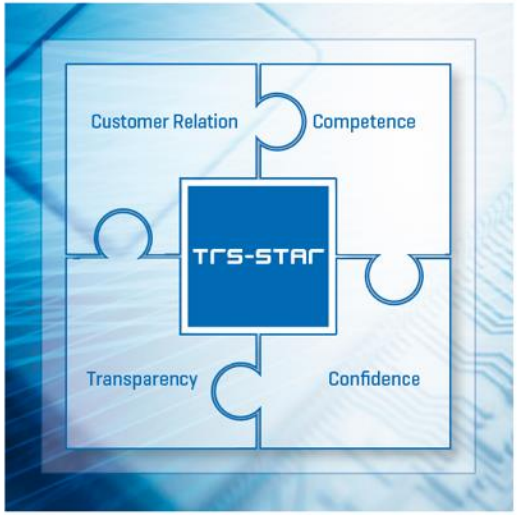

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